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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,559	07/22/2003	Yoshihisa Iwata	240522US2S	6040

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EXAMINER	
TAN, VIBOL	
ART UNIT	PAPER NUMBER
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/19/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/623,559	IWATA, YOSHIHISA	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-14,23 and 24* is/are allowed.

6)☒ Claim(s) *16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 21 and 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Buxton et al. (U. S. PAT. 6,473,280).

In claim 21, Buxton et al. teaches all claimed features in Fig. 2, a semiconductor apparatus comprising a logic level decision circuit (44) to which a first reference signal (V_{high}) having a logic "1" level and a second reference signal (V_{low}) having a logic "0" level are input as reference signals for deciding a logic level (46) of an input signal having a binary logic (logic 1 or logic 0), and which decides the logic level of the input signal in accordance with which of the signal levels of the first and second reference signals the signal level of the input signal is close to, wherein the first and second reference signals (V_{high} and V_{low}) are inputted from outside (external) of the semiconductor apparatus (44).

In claim 22, Buxton et al. teaches all claimed features in Fig. 2, a semiconductor apparatus having a logic level decision circuit (44), the logic level decision circuit comprising: a first comparison circuit (upper comparator in 44) which compares an

external input signal (46) with a first reference signal (V_{high}) corresponding to logic "1" level, and which outputs a first differential signal (output from the upper comparator in 44); a second comparison circuit (lower comparator in 44) which compares the external input signal with a second reference signal (V_{low}) corresponding to logic "0" level, and which outputs a second differential signal (output from the lower comparator in 44); and a third comparison circuit (an AND circuit) which compares the output of the first comparison circuit and the output of the second comparison circuit, and which outputs one of the logic "1" level and the logic "0" level, wherein the output of the third comparison circuit follows the external input signal (46); an wherein the first and second reference signals are inputted from outside (external) of the semiconductor apparatus (44).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in Fig. 1 in view of Buxton et al.

In claim 16, the AAPA in Fig. 1 teaches a signal transmission system which transmits and receives binary logic signals (logic 1 and logic 0) between a plurality of semiconductor apparatuses (100s), wherein the plurality of semiconductor apparatuses respectively have an input receiver (101 in Fig. 1 of AAPA) that decides a logic level of

an external input signal (Vin); with the exception of teaching a first and a second reference voltages. However, Buxton et al. teaches in Fig 2, a first reference signal (V_{high}) corresponding to a logic "1" level of the input signal and a second reference signal (V_{low}) corresponding to a logic "0" level are supplied as reference signals for logic level decision (44) to the respective input receivers, and the respective input receivers output on of the logic "1) level and the logic "0" level, and the output of the respective input receivers follows the external signal (46); wherein the first and second reference signals are inputted from outside (external of 44) of the plurality of semiconductor apparatus.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of the AAPA in Figs 1 and 2 with the teachings of Buxton et al. in order to provide detection circuits that can be used for transmitting signals in semiconductor circuits such as memory devices.

In claim 17, the AAPA in fig. 1 further teaches the plurality of semiconductor apparatuses (100s) are packaged on a same wiring board (Fig. 1), and structure a semiconductor module (as seen in Fig. 1).

In claim 18, Buxton et al. further teaches the signal transmission system of claim 16, wherein each of the input receivers including: a first comparison circuit (upper comparator in 44) which compares an input signal (46) with a first reference signal (V_{high}) corresponding to logic "1" level, and which outputs a first differential signal (output from the upper comparator in 44); a second comparison circuit (lower comparator in 44) which compares the input signal (46) with a second reference signal (V_{low}) corresponding to logic

"0" level, and which outputs a second differential signal (output from the lower comparator in 44); and a third comparison circuit (an AND circuit) which compares output of the first comparison circuit and output of the second comparison circuit, and which decides a logic level (logic high or logic low) of the input signal.

In claim 19, Buxton et al. further teaches the signal transmission system according to claim 16, wherein a signal level (a voltage level) of the first reference signal (V_{high}) is greater (higher) than a signal level (a voltage level) of the second reference signal (V_{low}), and the signal level of the first reference signal is a value greater than a maximum value (highest voltage level for 46) of a distribution of a signal level of the logic "1" level of the input signal (46), and the signal level of the second reference signal is a value less than a minimum value (lowest voltage level) of a distribution of a signal level of the logic "0" level of the input signal (46).

Claim 20 is rejected in the same manner as claim 19, by reversing the first reference signals V_{high} and V_{low} around.

3. Claims 9-14, 23 and 24 appear to comprise allowable subject matter of the first comparison circuit is a current mirror type first voltage comparison circuit, and the second comparison circuit is a current mirror type second voltage comparison circuit.

Response to Arguments

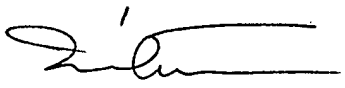
4. Applicant's arguments with respect to claims 16, 21 and 22 have been considered but are moot in view of the new ground(s) of rejection.

The new ground(s) of rejection has been set as discussed in detailed action above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



VIBOL TAN
PRIMARY EXAMINER